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Onboard data processing for Thermal-IR Imaging Spectrometer (TIS)

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Abstract: Thermal infra-red imaging spectrometer (TIS) is an imaging spectrometer flown onboard India's first Mars Orbiter Mission (MOM) along with four other instruments. It is a grating based spectrometer operating in 7µm to 13 µm (12 and 120 bands) spectral region, which makes use of an un-cooled micro-bolometer array as detector. TIS has spatial resolution of 250m (at perigee) and 55km (at apogee) from 372 x 80,000 km orbit of MOM. The instrument is configured to achieve low mass and low power which is a requirement. TIS consists of collimating optics, slit, grating and re-imaging optics, *160x120* element micro-bolometer and camera electronics. The camera electronics consists of power supply electronics, analog front end (AFE) electronics and digital control and processing electronics (DCPE). The AFE device processes the analog signal and digitizes to 16-bits. DCPE provides the control signals to the detector and to analog processing blocks. DCPE also receives the digitized data from the front-end electronics section and then performs real time data processing. The data processing includes byte to word conversion, pixel level oversampling and averaging, frame data accumulation (binning) for *4, 16* and *64* frames, spectral binning i.e. to convert *10:1* spectral compression, data formatting and then serialization of the data. All these processes are incorporated using an Field Programmable Gate Arrays (FPGA) along with an Static Random Access Memory (SRAM) with interface devices in a single miniaturized DCPE card. This paper gives the details of the onboard data processing and developments of DCPE for TIS instrument.

Keywords: Averaging, Binning, FPGA, Integration Time, SRAM, DCPE, AFE, Micro-Bolometer, SNR, Spectral band

1. Introduction

Thermal infra-red (IR) Imaging Spectrometer (TIS) is thermal imaging spectrometer flown onboard India's first Mars Orbiter Mission (MOM) along with four other instruments. TIS is a grating based spectrometer operating in 7µm to 13 µm (12 and 120 bands) spectral region, which makes use of an un-cooled micro-bolometer array as detector. TIS has a spatial resolution of 250m (at perigee) and 55km (at apogee) from 372 x 80,000 km orbit of MOM. It is aimed to achieve noise equivalent Δ-temperature of 1K at 300K target temperature. Micro-bolometer array as detector does not require cooling for its operation, unlike quantum IR detectors which operate usually at cryo-temperatures (Murphy, 2000; Pain and Fossum 1993). The thermal emission from Mars is expected to be low and the signal will almost be embedded in the background (radiation from detector surroundings). Thus to extract signal, dynamic range of the digitizer is required to be higher; so that Least Significant Bit (LSB) of the digitizer should commensurate with the signal level. Also, it is planned to carry out external binning digitally (in Field Programmable Gate Arrays - FPGA) to reduce the effect of random noise present in the detector and to increase the overall signal to noise ratio (Murphy, 2000; Joseph, 2005).

The instrument is configured to achieve low mass and low power which is a requirement and stringent objective for its realization that too within very short span of time. TIS consists of collimating optics, slit, grating and re-imaging optics, 160x120 element micro-bolometer and camera electronics. The block diagram of TIS is given in Fig.1. The camera electronics consists of power supply electronics, analog front end electronics (AFE) and digital control and processing electronics (DCPE). The AFEdevice processes the analog signal and digitizes to 16-bits. DCPE provides the control signals to the detector and to analog processing blocks. DCPE also receives the digitized data from the front-end electronics section and then performs real time data processing. The data processing includes byte to word conversion, pixel level oversampling and averaging, frame data accumulation (binning) for 4, 16 and 64 frames, spectral binning i.e. to achieve 10:1 spectral compression, data formatting and then serialization of the data. The details of these processes are given in the design description. All these processes are incorporated using an FPGA along with an SRAM with interface devices in a single miniaturized DCPE card. This paper gives the details of the onboard data processing and developments of DCPE for TIS instrument.

Camera electronics is custom designed for TIS, with goals to meet the functional and high performance requirements within the stringent constraints of minimum weight, size and power. The configuration is based on micro-Bolometer and system requirements. Overall camera electronics consists of regulated DC power supply, AFE for temperature controlling of the detector and true video extraction from detector output signal digitization, timing control and data processing

electronics circuits. The last two subsystems are DCPE.

The DCPE provides clocks and timings to the detector and front-end electronics for configuring the detector and operation of integrated digitizer (AFE). DCPE receives the AFE output data, which is available in Bit-parallel and Byte serial format and carries out all the data processing as per the mode selected. These operating modes are described in the next section.

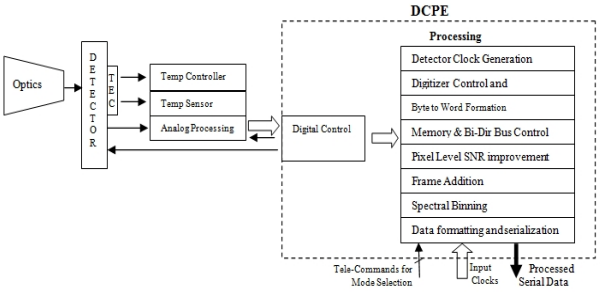

Figure 1: The diagram of Thermal infra-red (IR) Imaging Spectrometer (TIS)

2. Mode description

The micro-bolometer is being used for the first time onboard satellite by India. It has 160 x 120 array of thermistor elements optimized for sensing 7 to 13 µm IR radiation of optical region. The system developed around this detector requires stringent characterization and calibration. Also there are many uncertainties with respect to environment conditions, seasonal variations, orbital positions, signal strength during imaging in the perigee and apogee etc. Hence various test modes were incorporated in the TIS, to characterize the system, optimize the signal during available dwell time and also to reduce the output data volume. Table provides the summary of all modes with respect to the functional details explained in the subsequent sections.

Table 1: Mode description

Mode	AFE mode	Over sampling	Temp Monitoring	Spectral binning	Frame binning
1	Video Channel only	8	Nil	Nil	Nil
2A					4
2B					16
2C					64
3	2 Temp Channels with Video	2	Yes	10	Nil
4A					4
4B					16
4C					64

Dwell time of the space craft depends on its position with respect to Mars. Frame binning provision is kept to increase the resultant signal. Signal strength can be increased by multiple frames binning which in turn provides better SNR. Number of frames to be binned are kept programmable from 4, 16 to 64, which can be selected based on signal level of the object. This can be exercised during apogee imaging where relative movement of spacecraft with respect to MARS is very less. Fig. 2 depicts the frame binning concept.

Spectral binning provision is incorporated to facilitate reduction of data volume. This may be exercised based on target brightness as well as spectral interest of target feature. To reduce the total spectral bands, 10-consecutive band data (pixel wise) is accumulated and one single band is formed with wider bandwidth. With this signal strength will increase by a factor of 10; while the noise will increase by a factor of square root of 10. Thus the Signal-to-Noise Ratio (SNR) will improve by a factor of $\sqrt{10}$. Spectral binning will reduce spectral resolution but will improve signal strength and the SNR. The spectral binning concept is illustrated in Fig.3.

Figure 2: Frame binning concept illustrated

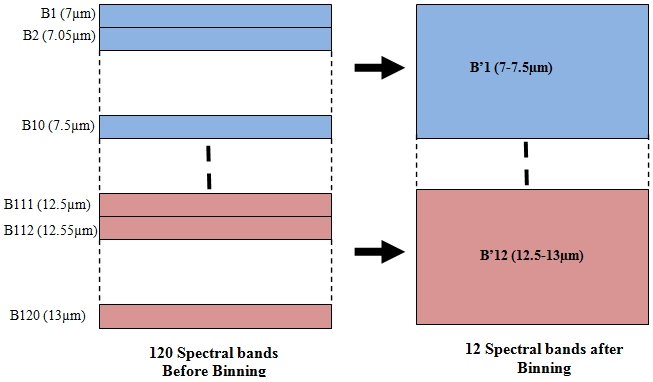

Figure 3: Spectral binning concept illustrated

As the background signal of the detector depends on the temperature of surrounding hardware (detector and head case) as well as its own temperature, in some of the modes (mode 3, 4A, 4B, 4C), AFE is configured in three channel mode where apart from video, other two channels of AFE (digitizer) take detector case temperature and internal case temperature signal and provide digital output which is inserted in the video data stream. This temperature information is used for background correction.

3. Realization

Considering the intricate and real time onboard data processing requirement, the usage of digital signal processors, FPGA and microcontrollers were looked into. Due to resource, power and space advantages,

FPGA and external SRAM based design is finalized. Logic design for TIS is carried out in VHDL (VHSIC Hardware Description Language) targeting available space grade and radiation tolerant *RT54SX32 (CQFP208)* FPGA having small package size. The FPGA has internal flip-flops with inbuilt TMR (Triple Module Redundancy). The inbuilt TMR removes the error caused by single event upsets (SEE – due to strong ionising space radiation), if any, in the flip-flops by majority voting. Thus, the chosen FPGA is immune to the SEE. Logic design is carried out as per the approved guidelines for FPGAs and has been thoroughly reviewed and verified by peer review team (Bhasker, 2010). Major challenge in the logic design is to accommodate all eight modes meeting functional requirements and complying to all design guidelines. Logic design contains following key features:

1. It generates detector clocks as per requirements
2. It facilitates oversampling by the AFE as per mode selection
3. It generates AFE timings for two different modes (single channel and 3 channel modes).
4. It controls SRAM such that within same pixel duration, *Read* and *Write* operations are performed during binning operations.
5. During spectral binning repetitive address sequence is generated for 10 lines.
6. Dual addressing of SRAM is carried out for data transmission as well as storing the current ADE data during spectral binning. This is done to avoid alternate frame data.
7. Logic also caters to bi-directional bus handling and avoids any bus-contention.

Major design parameters of DCPE are listed in Table-2.

Table 2: Major Design parameters of DCPE

S/N	PARAMETERS	SPECIFICATIONS
1.	No of Modes	8
2.	Detector Clocks	2
3.	Digitizer Clock	7
4.	Analog video rate	234 KHz
5.	Video Period	4.27 us
6.	Input Clock Rate	13.125 MHz
7.	One Frame Duration	83 ms
8.	Serial Data transmission rate	6.5625 Mbps

FPGA has to continuously communicate with SRAM for data exchange operations during frame and spectral binning. SRAM has 16-bit bi-directional data bus, on which data is communicated to FPGA and back to SRAM. Hence data bus handling in the FPGA becomes important and critical. The FPGA library has its bi-directional buffer (Actel Corporaion, 2009), which consists of a tri-state buffer and a normal buffer connected as shown in Fig.4.

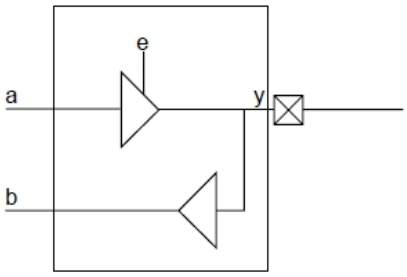

Figure 4: Bi-directional buffer in FPGA library

3.1 Digital control

DCPE receives master clock (Termed as Bit Rate Clock or BRC) of *13.125 MHz* and frame synchronizing pulse from the spacecraft. The BRC rate for the logic design is finalized based on following aspects (Joseph, 2005):

1. No. of elements to be read out in the detector in a frame time.
2. Detector requirements
3. SRAM timing requirements
4. Onboard processing requirements
5. Detector pixel duration
6. Final data rate for transmission and
7. Available crystal oscillator for master clock generation

Detector requires mainly two signals, namely *Clock* and a *Clear* pulse. Rate of the detector clock is seven times higher than the output pixel video rate. Clear pulse is frame rate pulse whose width should be around 2 µs (micro-seconds) as per detector requirements. Also first rising edge of the detector clock should be ahead of the clear falling pulse by > 200 ns. With these constraints the detector timings are generated and then provided to the detector.

AFE requires mainly two clocks for sampling and analog to digital conversion. First channel of the 3-channel AFE is connected to detector analog video while remaining two channels of AFE are connected to temperature sensors. When only one channel (analog output signal of the bolometer) is digitized the timings of the *AFE* are different than that of when all the three channels are digitized. Hence two different sets of the timings are generated for the AFE. There is also a requirement of oversampling of the analog video data to increase SNR. In this process, the analog video corresponding to each element of the detector is sampled more than once and then digitized.

3.2 Real time data processing

AFE's output is received by DCPE in 8-bit parallel, and 2-byte serial format which is reformatted to form 16-bit parallel data at DCPE. Averaging of these

samples of each pixel element is carried out in the FPGA to maintain *16-bit* data width.
As mentioned in the Table-1, this logic design is required to cater to total 8-modes. All these modes are programmable and selectable with *3-bits* level commands for mode selection, which will be received by DCPE from the spacecraft.

Mode-1 corresponds to raw data of full frame which will be transmitted continuously for each frame. After oversampling and averaging process, the data formatting is carried out and it is serialized as per selected mode.

Mode-*2a*, *2b* and *2c* of the FPGA logic design correspond to the full frame data binning. In this process, full frame *(160* elements of *120* bands) data of the bolometer is accumulated *n* times, where *n* is *4, 16 and 64* frames respectively, as per mode selection. The frame data is stored in the SRAM for *n* frames. During binning process, data is first read out from the memory and then added to the current frame data and then stored on the same location. For the first frame, read out data is ignored and current data is over-written in the SRAM. This ensures that no ambiguous data of the SRAM is considered immediately after power-on.

Mode-*3* corresponds to spectral binning only, where *10:1* band binned data is transmitted for each frame along with temperature information of the detector i.e. two remaining channels' data of AFE. Out of *120* original bands of the bolometer, *10* adjacent bands are converted into single aggregated band and the frame size reduces to *160 x 12*. The memory address generation becomes complex in this process as the data is to be read and written into the same locations for each of the new band formation. For example, each line consists of *160* elements. First *10* lines (bands) data is stored repetitively into the locations which correspond to *160* elements of the first aggregated band. The address sequence has to be repeated in such a way that, original *10*-bands *(160 x 10)* elements are accumulated on the same *160* locations. Here accumulation process consists of reading out from a memory location, addition of its content with the current pixel data and writing of the added data onto the same location. For each memory location, *Read-then-Write* sequence is followed (Prince, 2000). As soon as first *10*-bands data accumulation is completed, new address sequence is generated for second set of 10-bands, which again has to be repeated until *10*-bands data accumulation is over. During data transmission, when last frame data is read from the memory and then transmitted, acquisition of the current frame data is simultaneously going on. The address sequence for data transmission and for current data accumulation and binning is totally different, hence in the spectral binning case, dual addresses are generated for each location. As already mentioned, each memory location is divided into two timing zones, first for Read and second for Write operation. In the dual address mode, during Read timing zone, dual addresses were generated. First address corresponds to the location where spectrally binned data is stored, while second address belongs to the sequence for spectral-binning operation. When all spectrally binned data locations are covered, dual addressing mode stops and addresses become common. The data volume is reduced to $1/10^{th}$ after spectral binning process. Here all three channels of the AFE are digitized. Temperature data which is provided into two remaining channels of the AFE, is also available for each frame in this mode. The two channel's data is inserted into data stream after resultant *160 x 12* data is available.

Mode-*4a, 4b* and *4c* correspond to output data binning, spectrally as well as frame wise. In these modes along with the spectral binning, n-frame binning is also performed (where n is 4, 16 and 64). Data for n-frames are accumulated in the SRAM with the same principle of Read-then-Write. It is always ensured that after power-on or when first frame data is acquired, ambiguous SRAM data is read but ignored for the desired number of locations. It should be noted that during frame and spectral binning process, no of data bits increases from 16-bits to 26-bits. Since the SRAM configuration is of 16M (1M X 16 bits), two address locations are allotted for each element data read and write. Lower significant Word (LSW) or leftmost 16-bits are accumulated in a location and then More Significant Word (MSW) or upper remaining bits are accumulated in the next adjacent location of the SRAM. This helps to consider the carry bit(s) generated in the addition of stored LSW and current 16-bit data.

Since the valid data width in each mode is varying, data for each mode is formatted and serially transmitted to the spacecraft. Also, in case of binning modes, data will be in burst form, hence to indicate the valid data arrival to spacecraft, mode dependent auxiliary bits are inserted as header for each frame data.

4. Design verification

Extensive simulations of the logic design were carried out with manual test bench as well as automated test vector generation for different mode verification. As per guidelines, master clock frequency (or BRC) for design-synthesis was kept 16.4 MHz which is 25% higher than nominal clock rate of 13.125 MHz. Simulation is carried out with minimum, typical and maximum *SDF* (Standard Delay Format) timings with the help of *Questa-Sim* from Mentor Graphics. In addition simulation with various other combinations are also carried out, such as

1. 25% Faster clock
2. 25% Slower Clock
3. Nominal clock frequency with 40% and 60% duty cycle variation.

In all the cases SDF timings were varied from minimum, typical to maximum. Functionality is verified in terms of timing relations with respect to required specifications and found satisfactory throughout the simulations. Apart from FPGA in the DCPE card there are other interface devices like LVDS (Low Voltage Differential Signal) transmitter and receivers and a buffer. With these devices circuit analysis is also carried out like electrical stress analysis and Failure mode criticality analysis etc. All the simulations and design analysis were thoroughly reviewed by peer review teams as well as a top level reviewing committee. The design is approved to be implemented in flight model FPGA, for TIS (MOM) DCPE.

DCPE card is realized in 4-layer board of size 120mm x120mm. All active as well as passive components are Surface Mount Devices (SMD) to reduce the size and area of the card. Micro-D connectors are used for interfacing with other subsystems. The card requires single power supply line of +3.8V. It has an LDO (Low Drop-Out) regulator for generating +2.5V for FPGA core voltage. FPGA and memory are high power dissipating devices. To restrict the junction temperature of the devices to less than 110 ^{O}C even at the extreme condition of 55 ^{O}C in vacuum, thermal control measures are implemented like, incorporation of thermal vias (PTHs), Copper thickness of 70µm, maximization of Copper area, black painting of inside walls of the tray etc. The junction temperature for highest power dissipating device (SRAM device) is observed as ≈ 65 ^{O}C at ambient temperature of 55 ^{O}C in vacuum. To reduce EMI effects, following steps are followed (Bosshart, 2000; Ott, 1989).

- Circuit realization in MLB
- Care in layout to minimize parasitics
- High frequency clock interface using LVDS
- Packaging in tray which acts as Faraday cage
- Minimization of ground loops
- Maximization of PCB ground plane

Fig.5 shows the developed DCPE card for the TIS.

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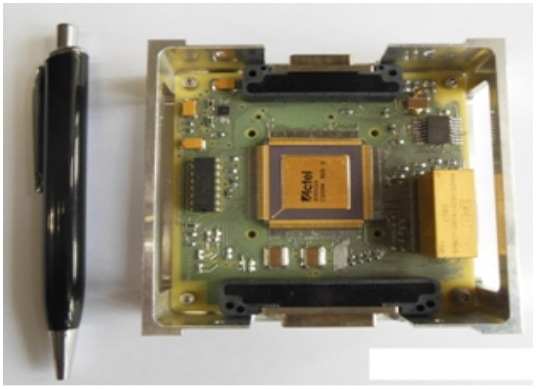

Figure 5: DCPE card in assembled package

DCPE card is realized in 4-layer board of size 120mm x120mm. All active as well as passive components are Surface Mount Devices (SMD) to reduce the size and area of the card. Micro-D connectors are used for interfacing with other subsystems. The card requires single power supply line of +3.8V. It has an LDO (Low Drop-Out) regulator for generating +2.5V for FPGA core voltage. FPGA and memory are high power dissipating devices. To restrict the junction temperature of the devices to less than 110 ^{O}C even at the extreme condition of 55 ^{O}C in vacuum, thermal control measures are implemented like, incorporation of thermal vias (PTHs), Copper thickness of 70µm, maximization of Copper area, black painting of inside walls of the tray etc. The junction temperature for highest power dissipating device (SRAM device) is observed as ≈ 65 ^{O}C at ambient temperature of 55 ^{O}C in vacuum. To reduce EMI effects, following steps are followed (Bosshart, 2000; Ott, 1989).

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6. Results and data verification

The circuit design with all the components was subjected to various design analysis (MIL-HDBK-217, 1995) and was reviewed by peer review team and approved for FM development. The flight model package of DCPE card is subjected to various environmental tests such as Initial Bench Test (namely, Nominal (+3.8V), incremental (+3.9V) and decremental power supply (+3.7V)), vibration, Thermo-Vacuum Cold soak and Hot soak, (-15°C to +55°C) and final bench test. All major test parameters such as power, signal levels, absolute and relative signal timings were verified along with the data verification in all programmable modes. All parameters were found within specified values. Since DCPE provides output data in serial form with separate format for 8 different modes, its data verification becomes a crucial task. To verify the data in each mode provision is made in the test setup to convert serial data to parallel and software is developed for data verification. Test setup consists of a stimulus generator, which is realized using a ProAsic FPGA. The stimulus generator simulates the output of the AFE used in the TIS front end circuit. It receives the conversion clocks from DCPE and generates the output data in bit parallel-byte serial form. The serial data is generated by incrementing a 16 bit counter such that it covers all the dynamic range. The 16 bits data is divided into two bytes and sent in the format similar to that of AFE used. The starting value of the counter is kept different for each mode of operation. Data generated by the DCPE is captured by the test setup and is compared with the data generated by test software. Data for all eight modes of operations is compared in the same manner. The design being synchronous, design specifications are specified in terms of master clock (BRC) cycles. The maximum acceptable aberration from the design specs is +/- 1 Master Clock Cycle. All the timing results found to be within specified tolerance limit.

7. Conclusion

An FPGA and SRAM based miniaturized (with respect to weight, size and power), digital processing and control electronics package is developed and its performance is found satisfactory, meeting all specifications at all phases of testing including integrated payload level tests. With this onboard processing, digitization from 16-bits to 26-bits is achieved meeting all functional requirements. SNR improvement is also achieved around 2.5 times (≈ 3.9 dB) after binning (from Mode-0 to Mode-3).

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